use and wherein the use registers and the self-refresh logic are implemented ~~adjacent to~~ in a same device as the memory cells;

wherein the memory device is configured to omit refreshing of memory cells that are not in use.

2. (Currently Amended) A memory device as recited in claim 1, ~~further comprising~~ wherein the self-refresh logic on the memory device ~~, wherein the self-refresh logic~~ is configured to not refresh the indicated unused memory cells.

3. (Original) A memory device as recited in claim 1, further comprising recent-access flags associated with respective sets of the memory cells, the recent-access flags being configured to indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory device is configured to omit refreshing of those memory cells that are indicated by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

4. (Original) A system comprising a plurality of memory devices as recited in claim 1, further comprising a memory controller configured to set the use registers to indicate whether the memory cells are unused.

5. (Currently Amended) A system comprising a plurality of memory devices as recited in claim 1, further comprising a memory controller implemented

on a different device than the use registers ~~configured to periodically refresh only those memory cells that are indicated by the use registers to be in use~~.

6. (Original) A system comprising a plurality of memory devices as recited in claim 1, further comprising a memory controller configured to cache at least some of those memory cells that are indicated by the use registers to be in use and to omit refreshing of the cached memory cells.

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7. (Original) A memory device as recited in claim 1, wherein the use registers comprise bits that each correspond to a set of memory cells.

8. (Original) A memory device as recited in claim 1, wherein the use registers comprise bits that each correspond to a row of memory cells.

9. (Original) A memory device as recited in claim 1, wherein the use registers comprise bits that each correspond to a bank of memory cells.

10. (Original) A memory device as recited in claim 1, wherein the use registers comprise bits that each correspond to a page of memory cells.

11. (Currently Amended) A memory device comprising:

a plurality of memory cells;

self-refresh logic to refresh the memory cells; and

one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are programmable to indicate whether the corresponding groups of memory cells are in use and wherein the use registers and the self-refresh logic are implemented ~~adjacent to~~ in a same device as the memory cells.

12. (Currently Amended) A memory device as recited in claim 11, ~~further comprising~~ wherein the self-refresh logic ~~on the memory device, wherein the self-refresh logic~~ is configured not to refresh unused memory cells.

13. (Original) A memory device as recited in claim 11, further comprising recent-access flags associated with respective sets of the memory cells, the recent-access flags being configured to indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory device is configured to omit refreshing of those memory cells that are indicated by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

14. (Original) A system comprising a plurality of memory devices as recited in claim 11, further comprising a memory controller configured to program the use registers depending on whether the memory cells are being used.

15. (Currently Amended) A system comprising a plurality of memory devices as recited in claim 11, further comprising a memory controller that is implemented on a different device than the use registers ~~configured to refresh only those memory cells indicated by the use registers to be in use~~.

16. (Original) A system comprising a plurality of memory devices as recited in claim 11, further comprising a memory controller that is configured to operate unused memory cells at reduced power.

17. (Original) A system comprising a plurality of memory devices as recited in claim 11, further comprising a memory controller configured to cache at least some of those memory cells whose use registers indicate they are not unused and to omit refreshing of the cached memory cells.

18. (Original) A memory device as recited in claim 11, wherein the use registers comprise bits that each correspond to a row of memory cells.

19. (Currently Amended) A system comprising:

one or more memory devices having dynamically refreshable memory cells;

a memory controller configured to periodically refresh the memory cells of the memory devices;

one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are

configurable to indicate whether the corresponding groups of memory cells are in use;

refresh logic on one of the memory devices configured not to refresh memory cells that are not in use; and

recent-access flags associated with the memory cells, the recent-access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory controller is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval,

wherein the refresh logic and the use registers are implemented on a same device as the memory cells.

20. (Currently Amended) A system as recited in claim 19, wherein the use registers are implemented on a different device than the memory controller ~~adjacent to the memory cells~~.

21. (Original) A system as recited in claim 19, wherein the memory controller is configured to cache at least some of those memory cells that are not indicated by the one or more use registers to be unused and to omit refreshing of the cached memory cells.

22-23. (Cancelled)

24. (Original) A system as recited in claim 19, wherein the use registers comprise bits that each correspond to a row of memory cells.

25. (Currently Amended) A system comprising:

memory including one or more memory cells;

a memory controller;

D1 an operating system configured to dynamically allocate and de-allocate the memory and to identify allocated and de-allocated memory to the memory controller; and

recent-access flags associated with the memory and implemented on a same device as ~~adjacent to~~ the memory cells, the recent-access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory controller is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval;

wherein the memory controller is responsive to the operating system to operate non-allocated memory at reduced power.

26. (Original) A system as recited in claim 25, wherein the memory is dynamically refreshable memory and the memory controller operates the non-allocated memory at reduced power by omitting refreshing of non-allocated memory.

27. (Canceled)

28. (Original) A system as recited in claim 25, wherein memory controller is configured to cache at least some of the allocated memory and to omit refreshing of the cached memory.

29. (Original) A system as recited in claim 25, further comprising a plurality of use bits corresponding respectively to memory rows, wherein each use bit being configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated.

30. (Original) A system as recited in claim 25, further comprising a plurality of use bits on the memory controller corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated.

31. (Original) A system as recited in claim 25, wherein the memory comprises a plurality of discrete memory devices, the system further comprising a plurality of use bits on the memory devices corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding

memory row is currently allocated, and wherein the memory controller configured to omit refreshing of memory rows that are not currently allocated.

32. (Currently Amended) In a system having dynamically refreshable memory rows, a method of memory power management, comprising:

keeping track of which memory rows are in use and therefore need refreshing;

periodically refreshing those memory rows that are in use;

omitting refreshing of memory rows that are not in use; and

determining which rows have been accessed in a manner that refreshed the memory rows during a previous refresh cycle interval, wherein the determining act is performed by utilizing a plurality of recent-access flags associated with each of the memory rows and implemented in a same device as ~~adjacent to~~ the memory rows.

33. (Previously Presented) A method as recited in claim 32, further comprising:

omitting refreshing of memory rows that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.

34. (Original) A method as recited in claim 32, further comprising:

caching at least some of the memory rows that are in use; and

omitting refreshing of the cached memory rows.

35. (Original) A method as recited in claim 32, wherein keeping track comprises maintaining a plurality of flags corresponding respectively to the memory rows.

36-37. (Canceled)

38. (Currently Amended) A memory controller configured to perform actions comprising:

periodically refreshing memory cells;

receiving notifications regarding which memory cells are in use based on data stored in a plurality of use registers;

omitting refreshing of those memory cells that are not in use; and

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval;

wherein the keeping track action is performed by utilizing a plurality of recent-access flags that are implemented adjacent to the memory cells,

wherein the memory controller is implemented in a different device than the use registers.

39. (Previously Presented) A memory controller as recited in claim 38, the controller being configured to perform further actions comprising:

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.

40. (Original) A memory controller as recited in claim 38, the controller being configured to perform further actions comprising:

caching at least some of the memory cells that are in use; and

omitting refreshing of the cached memory cells.

41-51. (Canceled)

52. (Currently Amended) A method comprising:

periodically refreshing memory cells;

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle,

wherein the period refreshing is performed by self-refresh logic and wherein the keeping track act is performed by utilizing a plurality of recent-access flags, the self-refresh logic being implemented ~~that are implemented adjacent to~~ on a same device as the memory cells.

53. (Original) A memory controller as recited in claim 52, further comprising:

receiving notifications regarding which memory cells are in use through a plurality of corresponding use registers; and

omitting refreshing of those memory cells that are not in use.

54. (New) A system as recited in claim 19, wherein the use registers are implemented on a different device than the memory controller.

55. (New) A system as recited in claim 25, wherein the memory cells are located on a different device than the memory controller.

56. (New) A system as recited in claim 29, wherein the use bits are implemented on a same device as the memory cells.

57. (New) A method as recited in claim 34, wherein a plurality of use registers are utilized to determine whether a memory row is in use and the use registers are implemented on the same device as the memory rows.

58. (New) A memory controller as recited in claim 38, wherein the use registers and the memory cells are implemented on a same device.

59. (New) A memory controller as recited in claim 53, wherein the use registers and the memory cells are implemented on the same device as the self refresh logic.